

WHAT IS CLAIMED IS:

1. A digitally controlled oscillator, comprising:
- 5 a preconditioner, wherein the preconditioner receives an input clock signal, wherein the preconditioner receives a master clock signal, wherein the preconditioner outputs a modified clock signal that is synchronized to the master clock signal; and
- a digital phase locked loop coupled to receive the modified clock signal output from the preconditioner, wherein the digital phase locked loop also receives the master
- 10 clock signal, wherein the digital phase locked loop outputs an output clock signal, wherein the output clock signal is a version of the input clock signal synchronized to the master clock signal;
- wherein the digital phase locked loop does not introduce phase noise to the synchronized version of the input clock signal.
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2. The digitally controlled oscillator of claim 1,
- wherein the preconditioner operates to noise shape phase noise of the synchronization to higher frequencies;
- wherein the digital phase locked loop operates to remove the phase noise at the
- 20 higher frequencies.
3. The digitally controlled oscillator of claim 2,
- wherein the preconditioner has a higher bandwidth than the digital PLL.
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4. The digitally controlled oscillator of claim 1,
- wherein the preconditioner includes a loop having a loop gain, wherein the loop gain operates to attenuate phase noise introduced internal to the preconditioner.

5. The digitally controlled oscillator of claim 1, wherein the preconditioner comprises:

a phase detector including a first input which receives the input clock signal and a second input, wherein the phase detector includes an output;

5 a loop filter having an input coupled to the output of the phase detector and including an output;

a voltage controlled oscillator (VCO) having an input coupled to the output of the loop filter and including an output;

10 a latch having an input coupled to the output of the VCO, an input which receives the master clock signal, and including an output which generates the modified clock signal, wherein the latch synchronizes the modified clock signal to the master clock signal, wherein the output of the latch is coupled to the second input of the phase detector to provide the modified clock signal to the phase detector.

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